CLAIMS

What is claimed is:

1. An integrated circuit fabricated on a chip, comprising:

an on-chip logic analyzer;

a cache memory that includes a plurality of cache sets;

at least one on-chip logic device that stores data to said plurality of cache sets during normal operation; and

a logic gate that receives an enable signal when the on-chip logic analyzer is enabled, and which disables at least one of said plurality of said cache sets for storing data from said on-chip logic analyzer.

2. The system of claim 1, wherein the integrated circuit comprises a processor, and the on-chip logic device includes a CPU core.

3. The system of claim 2, wherein the enable signal is generated by the on-chip logic analyzer.

4. The system of claim 3, wherein the logic comprises a multiplexer that connects the on-chip logic analyzer to the disabled cache set when the on-chip logic analyzer asserts the enable signal.

5. The system of claim 4, wherein the multiplexer forms part of a cache controller.

6. The system of claim 1, wherein the on-chip logic analyzer receives information regarding internal state data of the processor and selects some of the received information for storage in the disabled cache set.

7. The system of claim 6, further comprising a second on-chip logic analyzer that receives information regarding instructions executing in the processor, and wherein the second on-chip logic analyzer selects at least some of said received information for storage in the disabled cache set.

8. The system of claim 7, wherein the disabled cache set is sub-divided into multiple portions, and said on-chip logic analyzer and said second on-chip logic analyzer are each assigned a portion of said disabled cache set.

9. The system of claim 1, further comprising a cache controller that couples to said cache memory and which controls accesses to said cache memory, and wherein data stored by the on-chip logic analyzer is assigned an address range, and said cache controller forces a hit on said disabled cache set when a read request is made to the address range assigned to the on-chip logic analyzer.

10. The system of claim 1, wherein data stored by the on-chip logic analyzer is assigned an address range, and said disabled cache set makes available at least a portion of the data stored therein when a read request is made to the address range assigned to the on-chip logic analyzer.

11. The system of claim 10, wherein the on-chip logic analyzer includes an addressable read register that receives data stored in the disabled cache set in response to a read request to an address range assigned to the on-chip logic analyzer.

12. A processor, comprising:

a CPU core;

a cache memory coupled to said CPU core, said cache memory including a plurality of cache sets that during normal operation store data written by the CPU core; and

at least one logic analyzer that receives information relating to the internal state of the processor, said logic analyzer being coupled to at least one of said plurality of cache sets, and wherein said logic analyzer is capable of gaining ownership of said at least one cache set to store selected portions of said received information when said on-chip logic analyzer is enabled.

13. The processor of claim 12, further comprising a multiplexer that couples to said CPU core via a first bus and which couples to said logic analyzer via a second bus, and wherein said multiplexer selects either said first bus or said second bus to connect to said at least one cache set.

14. The processor of claim 13, wherein said multiplexer receives an enable signal indicating whether to connect said first bus or said second bus to said at least one cache set.

15. The processor of claim 13, wherein the logic analyzer is located on-chip.

16. The processor of claim 13, wherein said multiplexer couples to test logic via third bus, and wherein said multiplexer selects one of said first bus, said second bus, or said third bus to connect to said at least one cache set.

17. The processor of claim 16, wherein said multiplexer receives a first enable signal from said logic analyzer and a second enable signal from said test logic, and wherein said multiplexer selects which of said first, second or third bus to connect to said at least one cache set based on the status of said first and second enable signals.

18. The processor of claim 17, wherein said multiplexer awards priority to said logic analyzer if said logic analyzer requests access to said at least one cache set.

19. The processor of claim 12, wherein data stored by the logic analyzer is assigned an address range, and said at least one cache set makes available at least a portion of the data stored therein when a read request is made to the address range assigned to the logic analyzer.

20. The system of claim 19, wherein the logic analyzer includes an addressable read register that receives data stored in the at least one cache set in response to a read request to an address range assigned to the on-chip logic analyzer.

21. A processor fabricated on a chip, comprising:

a cache memory divided into a plurality of cache sets;

test logic coupled to said cache memory, which tests the cache sets during system initialization and determines which cache sets are operative;

a cache controller that controls the storage and retrieval of data from said cache memory, with said cache controller only storing data to cache sets that are determined to be operative by the test logic;

a CPU core coupled to said cache memory, said CPU core storing data to all operative cache sets during normal operation;

an on-chip logic analyzer capable of receiving data reflecting the internal state of the processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use by the CPU core when the on-chip logic analyzer is enabled.

22. The processor of claim 21, wherein data stored by the on-chip logic analyzer is assigned an address range, and said cache controller forces a hit on said disabled cache set when a read request is issued to the address range assigned to the on-chip logic analyzer.

23. The processor of claim 22, wherein the on-chip logic analyzer includes an addressable read register that receives data stored in the disabled cache set in response to the read request to an address range assigned to the on-chip logic analyzer.

24. The processor of claim 21, wherein the on-chip logic analyzer is capable of issuing a read request to the cache controller for data stored in the disabled cache set, which includes a signal indicating that the cache controller should force a hit on the disabled cache set.

25. A method of maintaining state data of a processor in a cache memory set, comprising the acts of:

enabling an on-chip logic analyzer to receive and select data for storage;

disabling a cache set from use by any device other than the on-chip analyzer;

storing said selected data in the disabled cache set.

26. The method of claim 25, further comprising the acts of:

reading said selected data from said disabled cache set; and

storing said data read from the disabled cache set to an addressable register.

27. The method of claim 25, wherein the act of disabling the cache set includes transmitting an enable signal to a multiplexer that selects the on-chip logic analyzer as the sole source of data to be written to the cache set.

28. The method of claim 26, wherein the act of reading selected data includes:

issuing a read request to an I/O address reserved for on-chip logic analyzer data;

recognizing the read request as targeting on-chip logic analyzer data;

routing the read request to the cache memory; and

forcing a hit on the disabled cache set.

29. The processor of claim 17, wherein said test logic will preserve the contents of at least one said cache set during a reset operation if said first enable signal is asserted.